REMARKS

In the Office Action, the examiner rejected Claims 1, 2 and 5-8 under 35 U.S.C. 102(b) as being anticipated by Testa et al. (cited reference U.S. Patent No. 5,845,234). Accordingly, the applicant has amended the claims to more clearly differentiate the features of the present invention from the technology disclosed by the cited Testa et al. reference.

As defined in the claims as amended, one of the essential features of the present invention resides in the fact that the comparison between the template and the constituent event is made at different levels of abstraction determined in advance, in the order of a signal level, a wavekind level where the signal is configured by a plurality of wavekinds, and a character level where the wavekind is configured by a plurality of characters. This feature is supported by the description from page 11, line 31 to page 15, line 24 with reference to Figures 10A-10B, 11 and 12. The present invention provides a technique for pre-optimization of tester resources use. The treatment of the mapping process in a hierarchical manner (signal, wavekind and character) is designed to minimize the number of timesets required during timeset formation.

In the system of the cited Testa et al. reference seems to employ an algorithm for timeset collapsing (from column 10, line 51 to column 11, line 49). The substantial difference is that the cited Testa et al. reference appears to relegate this step completely to the end of the process whereas the present invention

takes measures during initial mapping to optimize this post processing step. As timeset resources are known limitations on present-day semiconductor test systems, the applicant feels that this difference is significant.

With regard to claim 6, the claimed invention supports a common practice in the semiconductor test industry known as "pattern multiplexing". In this technique, a given tester cycle (or period) is divided into sub-cycles for the sole purpose of sharing the resources of a given pin across the sub-cycles. This allows the generation of more complex waveforms than might be allowed if the cycle were not split. The decision as to whether to apply this technique lies completely within the software as an automated step, and need not be initiated by the user. In by the cited Testa et al. reference, the applicant does not see any similar automated procedure or any precursor techniques from which the present invention might reasonably be derived.

With regard to claim 7, the claimed supports a common practice in the semiconductor test industry known as "pin multiplexing". In this technique, the resources of several pins are brought together to supply a single device pin. This allows more resources (driver/comparator edges) to be brought to bear on this signal allowing the generation of more complex waveforms. The decision as to whether to apply this technique lies completely within the software as an automated step, and need not be initiated by the user. Testa states "Each multiplexed group 50A is a grouping of

two or more signals which are grouped together to show combined signal information" (column 7, lines 5-10). This statement is quite general, and the techniques used to determine when such a technique is to be used are not presented in the cited Testa et al. reference. In light of this, the actual treatment of this technique (beyond a simple statement) disclosed in the instant case represents new and novel invention.

As discussed above, the present invention is distinguishable from the technology disclosed by the cited Testa et al. reference. Therefore, Applicant believes that the rejection under 35 U.S.C. 102(b) is no longer applicable to the present invention.

In this opportunity, the applicant has amended the specification to correct minor wording errors therein. This is to verify that no new matter has been introduced by the amendment.

In view of the foregoing, the applicant believes that 1 and 3-8 are in condition for allowance, and respectfully requests that the present application be allowed and passed to issue.

Respectfully submitted,

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